IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

1. (currently amended) A method of chained switching execution of data processing tasks, comprising:

~~storing a second return address corresponding to a second data processing task and a third return address corresponding to a third data processing task in a register;~~

executing a third data processing task until a task switching opportunity occurs;

calling a task switching function with the third data processing task to store a context of a second data processing task in a register when the task switch opportunity occurs;

executing the second data processing task until a second task switching opportunity occurs;

calling the task switching function with the second data processing task to store the context of the second data processing task linked ahead of the context of the third data processing task in the register when the second task switching opportunity occurs:

executing a first data processing task ~~executing a call to a task switching function~~;

executing a return call to the task switching function with the first data processing task;

~~the task switching function~~ selecting ~~the~~a ~~second return address or the third~~ return address from the register~~;~~ based on the return call with the task switching function while maintaining the storage of the second return address; and

~~the task switching function~~ executing a return operation to the data processing task corresponding to the selected return address with the task switching function.

2. (original) The method of Claim 1, wherein said selecting step includes the task switching function selecting a first pointer that points to a first area of memory where said return address is stored.

3. (original) The method of Claim 2, wherein said pointer selecting step includes updating a second pointer to point to said first pointer.

4. (original) The method of Claim 3, wherein said updating step includes updating the second pointer from a status wherein the second pointer points to a third pointer to a status wherein the second pointer points to said first pointer, and wherein said third pointer points to a second area of memory.

5. (original) The method of Claim 4, wherein a return address corresponding to said first data processing task is stored in said second area of memory.

6. (original) The method of Claim 5, including the task switching function storing said third pointer.

7. (original) The method of Claim 1, including the task switching function deselecting a return address corresponding to the first data processing task.

8. (original) The method of Claim 1, including saving a return address corresponding to the first data processing task, and executing said saving step in parallel with said call executing step.

9. (original) The method of Claim 1, wherein said first data processing task is one of a host task, a disk task and a servo task of an optical drive control system, and wherein the second data processing task is another of said host task, said disk task and said servo task.

10. (cancelled)

11. (currently amended) An apparatus for chained switching execution of tasks on a data processor, comprising:

a memory having a first storage location for storing a return address corresponding to a second task and a second storage location for storing a return address corresponding to a third task, wherein the first storage location is linked ahead of the second storage location;

an input for receiving information indicative of instructions of a task switching function

that has been called by a first task;

a memory management apparatus coupled to said input and said memory, and responsive to said instruction information indicating a return instruction for moving said return address from said ~~first storage location or said~~ second storage location to a register of the data processor while maintaining the first storage location in memory; and

wherein said data processor executes a return operation to the task corresponding to the return address stored in the register of the data processor.

12. (original) The apparatus of Claim 11, wherein said memory includes a second storage location for storing a first pointer which points to a first area of said memory that includes said first storage location, said memory management apparatus responsive to said instruction information for selecting said first pointer.

13. (original) The apparatus of Claim 12, wherein said memory management apparatus includes a memory manager for maintaining a second pointer, said memory manager responsive to said instruction information for updating said second pointer to point to said first pointer in said memory.

14. (original) The apparatus of Claim 13, wherein said memory manager is operable for updating said second pointer from a status wherein said second pointer points to a third pointer stored at a third location in said memory to a status wherein said second pointer points to said first pointer, and wherein said third pointer points to a second area of said memory.

15. (original) The apparatus of Claim 14, wherein said second area of said memory includes a fourth storage location which stores therein a return address corresponding to said first data processing task.

16. (original) The apparatus of Claim 15, wherein said memory manager is responsive to said instruction information for storing said third pointer in said third location of said memory.

17. (currently amended) A data processing apparatus, comprising:

a data processing portion for executing data processing tasks;

a task switcher coupled to said data processing portion for switching from execution of a first task to execution of a second task or a third task, said task switcher including a memory having a first storage location for storing a return address corresponding to the second task, and a second storage location for storing a return address corresponding to the third task, wherein the first storage location is linked ahead of the second storage location, and an input for receiving information indicative of instructions of a task switching function that has been called by the first task;

a register coupled to said task switcher;

said task switcher including a memory management apparatus coupled to said input and said memory, and responsive to said instruction information indicating a return instruction for moving said return address from said ~~first storage location or said~~ second storage location to a register of the data processing apparatus while maintaining the first storage location in memory; and

the task switcher switching from execution of the first task to execution of the task corresponding to the return address stored in the register of the data processing apparatus.

18. (original) The apparatus of Claim 17, wherein said task switcher includes a portion of a TriCore data processor architecture.

19. (original) The apparatus of Claim 17, wherein said register is a program counter register.

20. (original) The apparatus of Claim 17, wherein said first data processing task is one of a host task, a disk task and a servo task of an optical drive control system, and wherein the second data processing task is another of said host task, said disk task and said servo task.